BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Japanese Patent Laid-Open Publication No. Heisei 9-8205

[TITLE OF THE INVENTION]

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

[CLAIMS]

1. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and

terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond a resin encapsulate, each inner lead possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising:

inner leads having the thickness less than that of the lead frame blank; and

terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1511 to be electrically connected to the associated circuits, inner leads 1512 formed integrally with the outer leads 1513, bonding wires 1530 for electrically connecting the tips of the inner leads 1512 to the bonding pad 1521 of the semiconductor chip 1520, and a resin 1540 encapsulating the semiconductor chip 1520 to protect the semiconductor chip 1520 from external stresses and contaminants. This resin-encapsulated semiconductor device, after mounting the semiconductor chip 1520 on the bonding pad 1521, is manufactured by encapsulating the semiconductor chip 1520 with the resin. In this resin-encapsulated semiconductor device, the number of the inner leads 1512 is equal to that of the bonding pads 1521 of the semiconductor chip 1520. And, FIG. 15(b) shows the configuration of a monolayer lead frame used as an assembly member of the resin-encapsulated semiconductor device shown in FIG. 15a. Such a lead frame includes the bonding pad 1511 for mounting the semiconductor chip, the inner leads 1512 to be electrically connected to the semiconductor chip, the outer lead 1513 which is integral with the inner leads 1512 and is to be electrically connected to the associated circuits. This also includes dam bars 1514 serving as a dam when encapsulating the semiconductor chip with the resin, and a frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy(a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the line F1-F2 of FIG. 15(b)(A).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, particularly quad plate package(QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages ar fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for forming semiconductor packages having a large number of

pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1010 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1020 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).

Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100% of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80 □m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.
mm.

However, recent miniature resin-encapsula
semiconductor package requires inner leads arranged
pitches in the range of 0.13 to 0.15 mm, far smaller th
0.165 mm. When a lead frame is fabricated by processing
thin sheet of a reduced thickness, the strength of t
outer leads of such a lead frame is not large enough
withstand external forces that may be applied thereto
the subsequent processes including an assembling proce
and a chip mounting process. Accordingly, there is a lim
to the reduction of the thickness of the thin sheet t
enable the fabrication of a minute lead frame having fin
leads arranged at very small pitches by etching.

An etching method previously proposed to overcom
such difficulties subjects a thin sheet to an etchin
process to form a lead frame after reducing the thickness
of portions of the thin sheet corresponding to the inner
leads of the lead frame by half etching or pressing to form
the fine inner leads by etching without reducing the
strength of the outer leads. However, problems arise in
accuracy in the subsequent processes when the lead frame is
formed by etching after reducing the thickness of the
portions corresponding to the inner leads by pressing; for
example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting proc ss. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in assoc
position shift and coplanarity of an outer lead.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

According to one aspect of the present
there is provided a resin-encapsulated semiconduc
using a lead frame which is shaped in accordan
two-step etching process to a body wherein a thi
inner leads is less than that of the lead fra
comprising: inner leads having the thickness less
of the lead frame blank; and terminal columns
connected to the inner leads and having the same
with the lead frame blank, the terminal columns pc
a column-shaped configuration which is adapted
electrically connected to an external circuit, the
columns being disposed outside of the inner lea
manner such that they are coupled to the inner lea
direction orthogonal to the thickness-wise di
thereof, the terminal columns having terminal p
arranged on top ends thereof, the terminal portion
made of solders, etc. and exposed to the outside be
resin encapsulate, outer surfaces of the terminal
also being exposed to the outside beyond the
encapsulate, each inner lead possessing a recta
cross-section and having four surfaces including a

surface, a second surface, a third surface and a fo
surface, the first surface being flushed with one surf
of a remaining portion of the inner lead having the s
thickness with the lead frame blank while being opposed
the second surface, and each of the third and fou
surfaces having a concave shape depressed toward the ins
of the inner lead.

According to another aspect of the present inventio
there is provided a resin-encapsulated semiconductor dev
using a lead frame which is shaped in accordance with
two-step etching process to a body wherein a thickness
inner leads is less than that of the lead frame blan
comprising: inner leads having the thickness less than tha
of the lead frame blank; and terminal columns integrall
connected to the inner leads and having the same thickne
with the lead frame blank, the terminal columns possessin
a column-shaped configuration which is adapted to b
electrically connected to an external circuit, the termina
columns being disposed outside of the inner leads in a
manner such that they are coupled to the inner leads in a
direction orthogonal to the thickness-wise direction
thereof, portions of top ends of the terminal columns being
exposed to the outside beyond a resin encapsulate, outer
surfaces of the terminal columns also being exposed to the
outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

According to another aspect of the present invention, a semiconductor chip is received inward of the inner leads, and electrodes (pads) of the semiconductor chip are electrically connected to the inner leads through wires, respectively. According to another aspect of the present invention, the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad. According to another aspect of the present invention, the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape. According to still another aspect of the present invention, the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

[WORKING FUNCTIONS]

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and colplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

[EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance

with a first embodiment of the present invention described hereinafter with reference to FIGs. 1 FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention.. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional vie terminal column taken along the line B1-B2 of FIG. Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a view of the resin-encapsulated semiconductor device o 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In F and 2, a drawing reference numeral 100 represents a encapsulated semiconductor device, 110 a semicond chip, 111 electrodes (pads), 120 wires, 130 a lead f 131 inner leads, 131Aa a first surface, 131Ab a s surface, 131Ac a third surface, 131Ad a fourth surface terminal columns, 133A terminal portions, 133B surfaces, 133S a top surface, 135 a die pad, and 1 resin encapsulate.

In the resin-encapsulated semiconductor d according to the first embodiment, as shown in FIG. the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 133 at the surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131Bt of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133A located on the top surfaces 133S of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 5(a) is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 □m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire boding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the inner leads 131 is long or not. The inner leads having the contour, as shown in FIG. 9(a), in which the tips of the inner leads 131 are separated one from another, are prepared by the etching process, and the inner leads are resin-encapsulated after mounting the semiconductor chip thereon as will be described later. However, where the inner leads 131 are long in their length and have a tendency for the generation of twisting therein, it is impossible to fabricate the lead frame by etching to have the contour as shown in FIG. 9(a). Therefore, after etching the lead frame in a state where the tips of the inner leads are fixed to the connecting portion 131B as shown in FIG. 9(c)(イ), the inner leads 131 are fixed with the reinforcing tape 160 as shown in FIG. 9(c)(ロ). Then, the connecting portions 131B which are not necessary in the fabrication of the resin-encapsulated semiconductor device are removed by a press as shown in FIG. 9(c)(ハ), and a semiconductor device is then mounted on the lead frame.

Hereinafter, a method for the fabrication of the resin-encapsulated semiconductor device will now be described with reference to FIG. 8. First, the lead frame 130A, as shown in FIG. 9(a), which is shaped by the etching process as will be described later, is prepared such that the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131Ab of the inner leads 131 are bonded with each other using wires 120 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press to form terminal columns 133 and also the side surfaces 133B of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the resultant structure in such a manner that the side surfac s

of the terminal columns 133 are covered thereby FIG. 8(f)). At this time, the protective frame 180 functions to reinforce the semiconductor device. In other words, the protective frame 180 serves to prevent moisture from leaking into a gap between the resin encapsulate and the terminal columns due to the fact that the side surfaces of the terminal columns are exposed to the outside, whereby a crack is not formed in the semiconductor device and the breakage of the semiconductor device is avoided. However, persons skilled in the art will readily appreciate that it is not necessarily required to provide the protective frame 180. Also, when such an encapsulating process by the resin is carried out using a desired mold, the encapsulating process is implemented in a state wherein the outer side surfaces of the terminal columns of the lead frame are somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first embodiment will now be described in conjunction with the attached drawings. FIG. 11 is of cross-sectional views respectively illustrating sequential steps of the etching process for the lead frame of the first embodiment. In particular, the cross-sectional views of FIG. 1 correspond to a cross section taken along the line D1-D2 of FIG. 9(a). In FIG. 11, the reference numeral 1110 denotes a lead frame blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1161 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride solution of a temperature of 57℃ at a spray pressure of

2.5 kg/cm^2. The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth h corresponding to t/3 of the thickness of the lead frame blank (FIG. 11 c).

Although both surfaces of the lead frame blank 1111 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. 11(c)).

It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that the etch-resistant layer 1180 be coated over the entir

portion of the surface formed with the first recesse
and first opening 1130, as shown in FIG. 11(c), beca
is difficult to coat the etch-resistant layer 1180 c
the surface portion including the first recesses
Although the etch-resistant layer 1180 wax employed i
embodiment is an alkali-soluble wax, any suitabl
resistant to the etching action of the etchant soluti
remaining somewhat soft during etching may be used.
for forming the etch-resistant layer 1180 is not limit
the above-mentioned wax, but may be a wax of a UV-se
type. Since each first recess 1130 etched by the pr
etching process at the surface formed with the pa
adapted to form a desired shape of the inner lead t
filled up with the etch-resistant layer 1180, it is
further etched in the following secondary etching proc
The etch-resistant layer 1180 also enhances the mechan
strength of the lead frame blank for the second etc
process, thereby enabling the second etching process t
conducted while keeping a high accuracy. It is
possible to enable a second etchant solution to be spr
at an increased spraying pressure, for example, 2.5 kg
or above, in the secondary etching process. The increa
spraying pressure promotes the progress of etching in
direction of the thickness of the lead frame blank in
secondary etching process. Then, the lead frame blank

subjected to a secondary etching process. In this secondary etching process, the lead frame blank 1110 is etched at its surface formed with first recesses 1150 having a flat etched bottom surface, to completely perforate the second recesses 1160, thereby forming the tips of inner leads 131A (FIG. 11(d)).

The bottom surface 1170 of each recess formed by the primary etching process is flat. However, both side surfaces of each recess positioned at opposite sides of the bottom surface 1170 have a concave shape depressed toward the inside of the inner lead. Then, the lead frame blank is cleaned. After completion of the cleaning process, the etch-resistant layer 1180, and resist films (resist patterns 1120A and 1120B) are sequentially removed. Thus, a lead frame 130A having a structure of FIG. 9(a) is obtained in which tips of the inner leads 131A are arranged at a fine pitch. The removal of the etch-resistant layer 1180 and resist films (resist patterns 1120A and 1120B) is achieved using a sodium hydroxide solution serving to dissolve them.

The processes for manufacturing the lead frame as shown in FIG. 11, is to form by means of etching the lead frame having the tips of the inner leads used in this embodiment of the present invention, which have a thickness less than that of the lead frame. Especially, the first

surfaces 131Aa of the tips of the inner leads as shown in FIG. 1, are flushed with one surfaces of remaining portions of the inner leads having the same thickness with the lead frame while being opposed to the second surfaces 131Ab, and the third and fourth surfaces are formed to have a concave shape which is depressed toward the inside of the inner leads. Where a semiconductor chip is mounted on the second surfaces 131Ab of the inner leads by means of bumps for an electrical connection therebetween, as in a semiconductor device according to a third embodiment as will be described hereinafter, an increased tolerance for the connection by bumps is obtained when the second surface 131Ab has a concave shape depressed toward the inside of the inner lead. To this end, an etching method shown in FIG. 12 is adopted in this case. The etching method shown in FIG. 12 is the same as that of FIG. 11 in association with its primary etching process. After completion of the primary etching process, the etching method is conducted in a manner different from that of the etching method of FIG. 11 in that the second etching process is conduced at the side of the first recesses 1150 after filling up the second recesses 1160 by the etch-resist layer 1180, thereby completely perforating the second recesses 1160. At this time, by implementing the primary etching process, etching at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 111Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness t of the inner lead tip which is finally obtained. For example, where the blank has a thickness t reduced to 50 □m, the inner leads can have a fineness corresponding to a lead width W1 of 100 □m and a tip pitch p of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness t of about 30 □m and a lead

width W1 of 70 □m, it is possible to form inner leads having a fineness corresponding to an inner lead pitch p of 0.12 mm. Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness t and the lead width W1. That is to say, an inner lead tip pitch p up to 0.08 mm, a blank thickness up to 25 □m , and a lead width W1 up to 40 □m can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(イ). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(イ) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 (a polyimide tape is generally used, as shown in FIG. 9(c)(A). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(B), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(イ)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width W1 slightly greater than the width W2 of an opposite surface. The widths W1 and W2 (about 100□m) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(□)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(二)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(八) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared to that of the etched flat surface of this first embodiment. FIG. 13(二) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(二). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(二)(a) or FIG. 13(二)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device, 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 212, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231Ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(イ), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(ロ), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGs. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(A)(b), both widths W1A and W2A (about 100 □m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(□)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line B7-B8 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 410 a semiconductor chip, 411 pads, 430 a-lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surfac , 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth embodiment, one surface of the semiconductor chip 410 on which the pads 411 are disposed is fastened to the second

surfaces 431Ab of the inner leads 431 by the insul adhesive 470, and the pads 411 and the first surfaces of the inner leads 431 are electrically connected with other by wires 420. The semiconductor device of fourth embodiment uses the same lead frame which is use the third embodiment, which has the contour as show FIG. 10(a) and 10(b). Also, in the case of this fo embodiment, as in the case of the first and sec embodiments, the electrical connection between the res encapsulated semiconductor device 400 of this embodim and an external circuit is achieved by mounting the res encapsulated semiconductor device 400 via the termi portions 433A each being made of a semi-spherical solde on a printed circuit substrate, with the terminal portio 433A located on the top surfaces of the terminal colum 433, respectively.

FIG. 7(d) is a cross-sectional view illustrating modified example of the semiconductor device in accordanc with the fourth embodiment of the present invention. I the modified example of the semiconductor device as show in FIG. 7(d), the terminal portions each comprising th semi-spherical solder are not provided, and the to surfaces of the terminal columns are directly used as th terminal portions. Because the protective frame is not used and the side surfaces 433B of the terminal columns 43

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

[EFFECTS OF THE INVENTION]

The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay time.

59:543 v1

(19)日本国特許庁（JP）　(11)公開特許公報（A）　(11)特許出願公開番号

特開平9－8205

(43)公開日　平成9年（1997）1月10日

(51)Int.Cl.*	識別記号	庁内整理番号	FI	技術表示箇所
H01L 23/50			H01L 23/50	J
23/12			23/12	L

審査請求　未請求　請求項の数7　FD　（全15頁）

(21)出願番号　特願平7－170490

(22)出願日　平成7年（1995）6月14日

(71)出願人　000002897
大日本印刷株式会社
東京都新宿区市谷加賀町一丁目1番1号

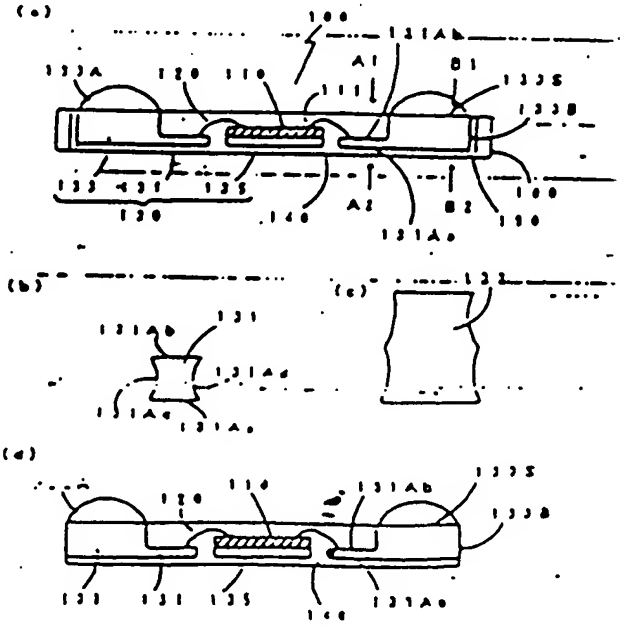
(72)発明者　山田　進一
東京都新宿区市谷加賀町一丁目1番1号
大日本印刷株式会社内

(72)発明者　佐々木　実
東京都新宿区市谷加賀町一丁目1番1号
大日本印刷株式会社内

(74)代理人　弁理士　小西　淳美

(54)【発明の名称】樹脂封止型半導体装置

(57)【要約】　(修正有)
【目的】　多ピン化に対応でき，且つ，アウターリードの位置ズレや平坦性の向上にも対応できる樹脂封止型半導体装置を提供する。
【構成】　一体的に連結したリードフレーム素材と同じ厚さの外部回路と接続するための凸状の端子部１３３とを有し，且つ，端子部はインナーリードの外部側においてインナーリードに対して厚み方向に屈曲して設けられており，端子部の先端面に半田等からなる端子部を設け，端子部を封止樹脂部から露出させ，端子部の外部側の側面を封止樹脂部から露出させており，インナーリードは，断面形状が略方形で第１面１３１Ａａ，第２面Ａｂ，第３面Ａｃ，第４面Ａｄの４面を有しており，かつ第１面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第２面に向き合っており，第３面，第４面にインナーリードの内側に向かって凹んだ段状に形成されている。



【特許請求の範囲】

【請求項1】　2段エッチング加工によりインナーリードの厚さがリードフレーム素材の厚さよりも薄肉に形成されたリードフレームを用いた半導体装置であって，前記リードフレームは，リードフレーム素材よりも薄肉のインナーリードと，該インナーリードに一体的に連なったリードフレーム素材と同じ厚さの外部回路と接続するための広巾の端子巾とを有し，且つ，端子巾にはインナーリードの外側側においてインナーリードに対して曲み方向に直交して設けられており，端子巾の先端部に半田等からなる端子玉を設け，端子玉を封止用樹脂層から露出させ，端子巾の外部側の側面を封止用樹脂層から露出させており，インナーリードは，断面形状が略方形で第1面，第2面，第3面，第4面の4面を有しており，かつ第1面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第2面に向き合っており，第3面，第4面はインナーリードの内側に向かって凹んだ形状に形成されていることを特徴とする樹脂封止型半導体装置。

【請求項2】　2段エッチング加工によりインナーリードの厚さがリードフレーム素材の厚さよりも薄肉に形成されたリードフレームを用いた半導体装置であって，前記リードフレームは，リードフレーム素材よりも薄肉のインナーリードと，該インナーリードに一体的に連なったリードフレーム素材と同じ厚さの外部回路と接続するための広巾の端子巾とを有し，且つ，端子巾にはインナーリードの外側側においてインナーリードに対して曲み方向に直交して設けられており，端子巾の先端の一部を封止用樹脂層から露出させて端子玉とし，端子巾の外部側の側面を封止用樹脂層から露出させており，インナーリードは，断面形状が略方形で第1面，第2面，第3面，第4面の4面を有しており，かつ第1面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあって第2面に向き合っており，第3面，第4面はインナーリードの内側に向かって凹んだ形状に形成されていることを特徴とする樹脂封止型半導体装置。

【請求項3】　請求項1ないし2において，半導体素子はインナーリード側に位置し，該半導体素子の電極部にワイヤにてインナーリードと電気的に接続されていることを特徴とする樹脂封止型半導体装置。

【請求項4】　請求項3において，リードフレームにダイパッドを有しており，半導体素子はダイパッド上に接着され，固定されていることを特徴とする樹脂封止型半導体装置。

【請求項5】　請求項3において，リードフレームにダイパッドを持たないもので，半導体素子はインナーリードとともに耐熱固定用テープにより固定されていることを特徴とする樹脂封止型半導体装置。

【請求項6】　請求項1ないし2において，半導体素子は半導体素子の電極側の面をインナーリードの第2面に絶縁性接着材により固定されており，該半導体素子の電極部はワイヤによりインナーリードの第1面と電気的に接続されていることを特徴とする樹脂封止型半導体装置。

【請求項7】　請求項1ないし2において，半導体素子はバンプによりインナーリードの第2面に固定されて電気的にインナーリードと接続していることを特徴とする樹脂封止型半導体装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は，半導体装置の多ピン化に対応でき，且つ，アウターリードの位置ズレ（スニュー）やアウターリードの平坦性（コプラナリティー）の向上に対応できる，リードフレームを用いた樹脂封止型半導体装置に関する。

【0002】

【従来の技術】従来より用いられている樹脂封止型の半導体装置（プラスチックリードフレームパッケージ）は，一般に図15（a）に示されるような構造であり，半導体素子1520を搭載するダイパッド部1511や他の回路との電気的接続を行うためのアウターリード部1513，アウターリード部1513に一体となったインナーリード部1512，該インナーリード部1512の先端部と半導体素子1520の電極パッド1521とを電気的に接続するためのワイヤ1530，半導体素子1520を封止してそれからの応力，湿気から守る樹脂1540からなっており，半導体素子1520もリードフレームのダイパッド1511部等に搭載した後に，樹脂1540により封止してパッケージとしたもので，半導体素子1520の電極パッド1521に対応できる数のインナーリード1512を必要とするものであろう。そして，このような樹脂封止型の半導体装置の独立部材として用いられる（単層）リードフレームは，一般には図15（b）に示すような構造のもので，半導体素子を搭載するためのダイパッド1511と，ダイパッド1511の周囲に設けられた半導体素子と接続するためのインナーリード1512，該インナーリード1512に接続して外部回路との接続を行うためのアウターリード1513，樹脂封止する際のダムとなるダムバー1514，リードフレーム1510全体を支持するフレーム（枠）部1515等を備えており，通常，コバール，42合金（42％ニッケル－鉄合金），銅系合金のような導電性に優れた金属を用い，プレス加工またはエッチング加工により形成されていた。尚，図15（b）（c）に，図15（b）（イ）に示すリードフレーム平面図のF1－F2における断面図である。

【0003】このようなリードフレームを利用した樹脂封止型の半導体装置（プラスチックリードフレームパッケージ）においても，電子機器の軽薄短小化の時代と半導体素子の高集積化には，小型薄型化かつ多ピン端子の

増大化が著しく、その結果、樹脂封止型半導体装置（特にQFP（Quad Flat Package）及びTQFP（Thin Quad Flat Package）等では、リードの多ピン化が著しくなってきた。上記の半導体装置に用いられるリードフレームは、微細なものにフォトリソグラフィー技術を用いたエッチング加工方法により作製され、微細でないものにプレスによる加工方法により作製されるのが一般的であったが、このような半導体装置の多ピン化にともない、リードフレームにおいても、インナーリード先端部の微細化が進み、当初は、微細なものに対しては、プレスによる打ち抜き加工によらず、リードフレーム素材の板厚が0．25mm程度のものを用い、エッチング加工で対応してきた。このエッチング加工方法の工程について以下、図14に基づいて簡単に述べておく。先ず、鉄合金もしくは42%ニッケル-鉄合金からなる厚さ0．25mm程度の母板（リードフレーム材料1410）を十分洗浄（図14（a））した後、重クロム酸カリウムを感光剤としたカゼインレジスト等のフォトレジスト1420を両面に同一に塗布する。（（図14（b））次いで、所定のパターンが形成されたマスクを介して両面同時にレジスト膜を露光した後、所定の現像液で未硬化なレジストを現像して（図14（c））、レジストパターン1430を形成し、硬膜処理、疎水処理等を必要に応じて行い、塩化第二鉄水溶液を主たる成分とするエッチング液にて、スプレイにて両面（リードフレーム材料1410）に穴を開け所定の寸法形状にエッチングし、貫通させる。（図14（d））……次いで、レジスト膜を剥離処理し（図14（e））、乾燥後、所定のリードフレームを得て、エッチング加工工程を終了する。このように、エッチング加工によって作製されたリードフレームに、更に、所定のエリアに金メッキ層が施される。次いで、必要な処理を経て、インナーリード部を固定用のポリイミド樹脂テープにてテーピング処理したり、必要に応じて所定のタブ吊りバーを曲げ加工し、ダイパッド部をダウンセットする処理を行う。しかし、エッチング加工方法においては、エッチング液による腐食は加工面のみならずその他に横（面）方向にも進むため、その微細化加工にも限度があるのが一般的で、図14に示すように、リードフレーム素材の両面からエッチングするため、ライン＆スペースの比率は、ライン幅/板厚の加工性は、通常、板厚の50～100%程度とされている。又、リードフレームのほこり等のアウターリードの強度を考えた場合、一般的には、その板厚は約0．125mm以上必要とされている。このため、図14に示すようなエッチング加工方法の場合、リードフレームの板厚を0．15mm～0．125mm程度まで薄くすることにより、ワイヤボンディングのための必要な巾寸法70～80μmを確保し、0．165mmピッチ程度の高密度なインナーリード先端のエッチングによる加工を達成してきたが、これが限度とされていた。

【0004】しかしながら、近年、樹脂封止型半導体装置は、小パッケージでは、多端子であるインナーリードのピッチが0．165mmピッチを見て、更に0．15～0．13mmピッチまでの狭ピッチ化要求がでてきたこと、エッチング加工において、リード先端の細工を細くした場合には、アセンブリ工程やまた工程といった後工程におけるアウターリードの強度確保が難しいという点から、単にリード部材の板厚を薄くしてエッチング加工を行う方法にも限界が出てきた。

【0005】これに対応する方法として、アウターリードの強度を確保した上で薄肉化を行う方法で、インナーリード部分をハーフエッチングもしくはプレスにより薄くしてエッチング加工を行う方法が提案されている。しかし、プレスにより薄くしてエッチング加工をおこなう場合には、後工程においての強度が不足する（例えば、めっきエリアの平滑性）、ボンディング、モールディング時のクランプに必要なインナーリードの平坦性、平面度が確保されない、等版を2度行なわなければならない等後工程が複雑になる、等問題点が多くある。そして、インナーリード部分をハーフエッチングにより薄くしてエッチング加工を行う方法の場合にも、等版を2度行なわなければならず、後工程工数が複雑になるという点があり、いずれも実用化には、未だ至っていないのが現状である。

【0006】

【発明が解決しようとする課題】一方、半導体装置の多端子化にともないインナーリードピッチが狭くなるに、半導体装置を実装する際に、アウターリードの位置ズレ（スキュー）や平坦性（コプラナリティー）の乱れ等が大きな問題となってきた。本発明は、このような状況のもと、多端子化に対応でき、且つ、アウターリードの位置ズレ（スキュー）や平坦性（コプラナリティー）の問題にも対応できる半導体装置の提供をしようとするものである。

【0007】

【課題を解決するための手段】本発明の樹脂封止型半導体装置は、2段エッチング加工によりインナーリードの一部がリードフレーム材料の厚さよりも薄肉に形成加工されたリードフレームを用いた半導体装置であって、前記インナーリードと、該インナーリードに一体的に連結したリードフレーム材料と同じ厚さの外部回路と接続するための主要の端子とを有し、且つ、該半導体チップのインナーリードの先端部においてインナーリードに対して略平行に延設して設けられており、該半導体チップの先端部に半田等からなる突起を設け、該半導体チップを封止樹脂層部から露出させ、該半導体チップの外部との接続を封止樹脂層部から露出させており、インナーリードに、断面形状が略方形で薄

1

180を設ける必要はなく，図1（d）に示すような位置に180を設けない構造のものでも良い．

【0010】実施例1の半導体装置100に使用のリードフレーム130は，42%ニッケル-鉄合金を素材としたもので，そして，図9（a）に示すような形状をした．エッチングにより外形加工されたリードフレーム130Aを用いたものであり，端子台部133部分や他の部分の厚さより薄肉に形成されたインナーリード部131をもつ．ダムバー136に樹脂封止する際のダムとなる．尚，図9（a）に示すような形状をした．エッチングにより外形加工されたリードフレーム130Aを，本実施例においては用いたが，インナーリード部131と端子台部133以外は最終的に不要なものであるから，特にこの形状に限定されない．インナーリード部131の厚さtは40μm，インナーリード部131以外の厚さtは0．15mmでリードフレーム素材の板厚のままである．インナーリード部131以外の板厚は0．15mmに限らず更に薄い0．125m～0．50mm程度でも良い．また，インナーリードピッチは0．12mmと狭いピッチで，半導体装置の多端子化に対応できるものとしている．インナーリード部131の第2面131Abは平坦状でワイヤボンディングしやすい形状となっており，図1（b）に示すように，第3面131Ac～第4面131-1Acにインナーリード側へ凹んだ形状もしており，第2面131Ab（ワイヤボンディング面）を狭くしても自由に設いものとしている．

【0011】本実施例においては，インナーリード13[illegible]の厚さが薄く，インナーリード131部にヨレが発生しやすい為，従来図9（a）に示すような，インナーリード先端がそれぞれ分離された形状のリードフレームをエッチング加工にして作製し，これに後述する方法により半導体素子を搭載して樹脂封止している．インナーリード132が広く，インナーリード131部にヨレを生じやすい場合には，従来図9（a）に示す形状にエッチング加工することに出来ないため，図9（c）-（イ）に示すようにインナーリード先端部を連結部131Bにて固定した状態にエッチング加工した後，インナーリード131部を粘着テープ160で固定し（図9（c）（ロ）），次いでプレスにて，半導体装置作製の際に不要の連結部131Bを除去し，この状態で半導体素子を搭載して半導体装置を作製する．（図9（c）（ハ））．

【0012】次に本実施例1の樹脂封止型半導体装置の製造方法を図8にもとづいて具体的に説明する．先ず，従来のエッチング加工にて外形加工された，図9（a）に示すリードフレーム130Aを，インナーリード131先端の第2面131Abが図8で上になるようにして用意した．（図8（a））．

次いで半導体素子110の電極111側の面を図8で上にして，半導体素子をダイパッド135上に搭載，固

(5)

2

定した．（図8（b））

半導体素子110をダイパッド135に固定した後，半導体素子110の電極111とインナーリード先端の第2面とをワイヤ120にてボンディングした．（図8（c））

次いで，従来の封止用金型：50で樹脂封止を行った後，不要なリードフレーム130の枠体150と接続していた部分をプレスにて切断し，図示しない端子台部133を形成するとともに端子台部133の側面133Bを形成した．（図8（d））

図9に示すリードフレーム130Aのダムバー136とフレーム枠137を除去した．この後，リードフレームの端子台の外側の面に半導体の一面からなる端子台133Aを形成して半導体装置を作製した．（図9（e））

次いで，従来は180を直接190を介して素子台の側面を覆うように，外周全体に設けた．（図8（f））尚，従来は：50に，半導体装置の端辺のみと，端子台の底面が接することにより封止金型と端子台の底面から樹脂が入り半導体装置にクランクが入り形成してしまうことがないようにするために設けたものであるが，必ずしも必要としない．また，樹脂による封止に所定の型を用いて行うが，半導体素子110のサイズで，且つ，リードフレームの端子台の外側の面が若干樹脂から外部へ突出した状態で封止した．

【0013】本発明の半導体装置に用いられるリードフレームの製造方法を以下，図にそって説明する．図11は，本実施例1のリードフレーム製造装置に用いられたリードフレームの製造方法を説明するための，インナーリード先端部をする装置における工程断面図であり，ここで作製されるリードフレームを示す平面図である図9（a）のD1-D2線の断面部における工程工程図である．図11e，1110はリードフレーム素材，1120Aは第一のレジストパターン，1120Bはレジストパターン，1130は第一の開口部，1140は第二の開口部，1150は第一の凹部，1160は第二の凹部，1170は半導体装置，180はエッチング処理面を示す．先ず，42%ニッケル-鉄合金からなり，厚さが0．15mmのリードフレーム素材1110の両面に，感光性感光液をスピンコート法により塗布した後，所定のパターンを有して，所定位置の第一の開口部1130，第二の開口部1140，1120Bを形成した．（図11（a））

第一の開口部1130は，次のエッチング加工においてリードフレーム素材1110とこの開口部からベタ状にリードフレーム素材よりも薄く加工するためのもので，レジストの第二の開口部1140は，インナーリード先端部の形状を形成するためのものである．第一の開口部1130は，少なくともリードフレーム1110のインナーリード先端部を形成するものが，本工程において，

て、テーピングの工程や、リードフレームを固定するクランプ工程で、ベタ状に露出された部分の近くなった区分との段差が問題になる場合があるので、エッチングを行うエリアはインナーリード先端の微細加工部分だけにとどまず大きめにとる必要がある。次いで、液温57°C、比重48ボーメの塩化第二鉄溶液を用いて、スプレー圧2.5kg/cm²にて、レジストパターンが形成されたリードフレーム素材1110の両面をエッチングし、ベタ状（平坦状）に露出された第一の凹部1150のほぼ中がリードフレーム素材の約2/3程度に達した時点でエッチングを止めた。（図11（b））

上記第1回目のエッチングにおいては、リードフレーム素材1110の両面から同時にエッチングを行ったが、必ずしも両面から同時にエッチングする必要はない。本実施例のように、第1回目のエッチングにおいてリードフレーム素材1110の両面から同時にエッチングする理由は、両面からエッチングすることにより、後述する第2回目のエッチング時間を短縮するためで、レジストパターン9208側からのみの片面エッチングの場合とくべ、第1回目エッチングと第2回目エッチングのトータル時間が短縮される。次いで、第一の凹部1150側の露出された第一の凹部1500にエッチング耐食層1180としての耐エッチングのあるホットメルト型ワックス（ブレンテック社製のワックス、型番MR-WB6）を、ダイコータを用いて、塗布し、ベタ状（平坦状）に露出された第一の凹部1150に埋め込んだ。レジストパターン1120Aとも耐エッチング耐食層1180に覆われた状態とした。（図11（c））

エッチング耐食層1180を、レジストパターン1120A上全面に塗布する必要はないが、第一の凹部1150をまたぐ一面にのみ塗布することに留意に、図11（c）に示すように、第一の凹部1150とともに、第一の貫口部1130側全面にエッチング耐食層1180を塗布した。本実施例で使用したエッチング耐食層1180は、アルカリ溶液のワックスであるが、基本的にエッチング液に耐性があり、エッチング時にある程度の粘性のあるものが、好ましく、特に、上記ワックスに限定されず、U.V.硬化型のものでもよい。このようにエッチング耐食層1180をインナーリード先端部の形状を形成するためのパターンが形成された面側の露出された第一の凹部1150に埋め込むことにより、後述するのエッチング時に第一の凹部1150が露出されて大きくなりすぎないようにしているとともに、耐食層はエッチング加工に対しての耐薬的な性質を有しており、スプレー圧を高く（2.5kg/cm²以上）とすることができ、これによりエッチングが広さ方向に進行しやすくなる。この後、第2回目のエッチングを行うベタ状（平坦状）に露出された第二の凹部1160形成面側からリードフレーム素材1110をエッチングし、貫通させて、インナーリード先端部1131Aを形成した。（図11（c））

第1回目のエッチング加工にて作製された、リードフレーム面に平行なエッチング形成面に形成してあるが、この面を底面2面にインナーリード側にへこんだ凹状である。次いで、洗浄、エッチング耐食層580の剥離レジスト膜（レジストパターン1120A、1120B）の剥離を行い、インナーリード先端部1131Aが形成されたリードフレーム130Aを得た。エッチング耐食層1a80とレジスト膜（レジストパターン1120A、1120B）の剥離に有機溶剤トリクロルエタンを超音波洗浄により同時に剥離した。

【0014】上記、図11に示すリードフレームの製造方法に、本実施例に用いられる、インナーリード先端部を両側に形成したリードフレームをエッチング加工により製造する方法で、特に、図1に示す、インナーリード先端の第1面131Aaを両側部以外の他の部分と同一面に、第2面131Abと対向させて形成し、且つ、第3面131Ac、第4面131Acをインナーリードの内側に向かって凹んだ形状にするエッチング加工方法である。上記する実施例3の手法は基板のようにバンプを用いて半導体チップをインナーリードの第2面131Abに接続し、インナーリードと電気的に接続する場合に、第2面131Abをインナーリード側に凹んだ形状に形成した方がバンプ接続の際の押圧荷重が大きくなる。図12に示すエッチング加工方法が採られる。図12に示すエッチング加工方法は、第1回目のエッチング工程までは、図11に示す方法と同じであるが、エッチング耐食層1180を第二の凹部1160側に埋め込んだ後、第一の凹部1150側から第2回目のエッチングを行い、貫通させて形成している。但し、第1回目のエッチングにて、第二開口部1140からのエッチングを充分に行っておく。図12に示すエッチング加工方法によって得られたリードフレームのインナーリード先端の断面形状は、図6（b）に示すように、第2面131Abがインナーリード側にへこんだ凹状になる。

【0015】尚、上記図11、図12に示すエッチング加工方法のように、エッチングを2段階にわけて行うエッチング加工方法を、一般には2段エッチング加工方法といっており、表面加工に有利な加工方法である。本発明に用いた図9（a）に示す、リードフレーム130Aのごとくにおいては、2段エッチングは不要で、パターン形状を工夫することにより部分的にリードフレーム素材を薄くしながらの形成加工をする方法とが採用されており、リードフレーム素材を薄くした部分においては、特に、微細な加工ができるようにしている。図11、図12に示す、上記の方法においては、インナーリード先端部131Aの微細化加工に、第二の凹部1160の形状と、最終的にはられるインナーリード先端部の厚さtに左右されるもので、例えば、厚さtを50μm

まで薄くすると、図11（c）に示す、平坦幅W1を100μmとして、インナーリード先端部ピッチpが0.15mmまで微細加工可能となる。板厚tを30μm程度まで薄くし、平坦幅W1を70μm程度とすると、インナーリード先端部ピッチpが0.12mm程度まで微細加工ができるが、板厚t、平坦幅W1のとり方次第ではインナーリード先端部ピッチpに更に狭いピッチまでの加工が可能となる。ちなみに、インナーリード先端部ピッチpを0.08mm、板厚25μmで平坦幅40μm程度が実現できる。

【0016】このようにエッチング加工にてリードフレームを作製する時、インナーリードの長さが短かい場合、或は工程でインナーリードのヨレが発生しにくい場合には、従来図9（a）に示す形状のリードフレームにエッチング加工にて作るが、インナーリードの長さが長く、インナーリードにヨレが発生し易い場合には、図9（c）（イ）に示すように、インナーリード先端部から連結部131Bを設け、インナーリード先端部にここに示した形状にして形成したものを用て、ここは本発明には不必要な連結部131Bをプレス等により切断除去して図9（a）に示す形状を得る。尚、前述のように、図9（c）（イ）に示すものを切断し、図9（a）に示す形状にする時には、図9（c）（ロ）に示すように、予め一時的のため保護テープ160（ポリイミドテープ）を仮貼する。図9（c）（ロ）の状態で、プレス等により連結部131Bを切断除去するが、本発明では、テープをつけた状態のままで、リードフレームに応力を与え、そのまま樹脂封止される。尚、E-E'、F-F'は切断部分を示すものである。

【0017】本実施例1の半導体装置に用いられたリードフレームのインナーリード部131の断面形状は、図13（イ）（a）に示すようになっており、ニッテング平坦面131Ab側の幅W1にはほぼ平坦で反対側の面の幅W2より若干大きくなっており、W1、W2（約100μm）ともこの部分の板厚と方向の幅Wよりも大きくなっている。このようにインリーリード先端部の断面は広くなった断面形状であるため、どちらの面においても半導体素子（図示せず）とインナーリード先端部131Aとワイヤ120A、120Bによる結線（ボンディング）が良いものとなっているが、本実施例の場合にはニッチング面側（図13（ロ）（a））をボンディング面としている。尚、131Abにニッチングによる平坦面、131Aaにリードフレーム平坦面121A、121Bにのっと当である。ニッチング平坦面がアラビの無い面であるため、図13（ロ）の（a）の場合は、特に結線（ボンディング）強度が強れる。図13（ハ）に従来14に示す加工方法にて作製されたリードフレームのインナーリード先端部13318と半導体素子（図示せず）との結線（ボンディング）を示すものであるが、この場合もインナーリード先端部13318の断面に平坦ではあるが、この部分の板厚方向の幅は大きくとれない。また両面ともリードフレーム平坦面であるため、結線（ボンディング）強度はニッチング平坦面より劣る。図13（ニ）にプレス（ニング）によりインナーリード先端部を扁平化したはにッチング加工によりインナーリード先端部133：C1331Dを加工したものの、ここは本発明に示すでとの結線（ボンディング）を示したものであるが、この場合にプレス圧力が図に示すように一定になっていたため、どちらの面を用いて結線（ボンディング）して6、図11（ニ）の（a）、（b）に示すように結線（ボンディング）の際に反応力が大きく品質的にも問題となる場合が多い。尚、1331Abにコイニング面である。

【0018】次に実施例1の樹脂封止型半導体装置の変形例を挙げる。図3（a）～図3（e）に、それぞれ、に実施例1の樹脂封止型半導体装置の変形例の断面図である。図3（a）に示す変形例の半導体装置に、実施例1の半導体装置とに、ダイパッド135の位置が異なるもので、ダイパッド部135が外部に露出している。ダイパッド135が外部に露出していることにより、実施例1にくべ、熱の発散性が優れている。図3（b）に示す変形例の半導体装置も、ダイパッド部135が外部に露出させているものであり、実施例1にくべ、熱の発散性が優れている。実施例1や図3（a）に示す変形例とに、半導体素子110の向きが異なり、ワイヤボンディング面をリードフレームの第1面に設けている。図3（c）、図3（d）、図3（e）に示す変形例に、それぞれ実施例1、図3（a）に示す変形例、図3（b）に示す変形例において、半導体の一辺からなる辺部を設けず、辺下巨の面を位置決手段として用いているものであり、樹脂二段を成形した構造となっている。

【0019】次いで、実施例2の樹脂封止型半導体装置を挙げる。図4（a）に実施例2の樹脂封止型半導体装置の断面図であり、図4（b）に図4（a）のA3－A4における断面図で、図4（c）は図4（a）のB3－B4における端子部の断面図である。尚、実施例2の半導体装置の外観は実施例1とほぼ同じとなる為、図は省略した。図中、200は半導体素子、211は電極部（パッド）、220はワイヤ、230はリードフレーム、231はインナーリード、231Aaは第1面、231Abは第2面、231Acは第3面、231Adは第4面、233は端子部、233Aは端子、233Bは側面、233Sは上端面、240は封止樹脂、270は熱硬化性テープある。この実施例2の半導体装置においては、リードフレーム230はダイパッドを持たないもので、半導体素子210にインナーリード231とともに熱硬化性テープ270により固定されており、半導体素子210は、半導体素子の電極部（パッド）211

例にワイヤ２２０により，インナーリード２３１の第２面２３１Ａｂとは接されている．本実施例２の場合も，実施例１場合と同様に，半導体基板２００と放熱板との電気的な接続は，吊下ピン２３３の先端部に設けられた半球状の半田からなる接手部２３３Ａを介してプリント基板等へ接続されることにより行われる．

【００２０】また，本実施例２の半導体装置は，図１０（ａ），１０（ｂ）に示す，ダイパッドを用たない，エッチングにより所定形状に加工されたリードフレーム２３０Ａを用いたもので，その製造方法に実施例１とほぼ同じ工程であるが，異なる点は，実施例１の場合には半導体チップをインナーリードに固定した状態でワイヤボンディングを行い，樹脂封止しているのに対し，本実施例２の場合には，半導体素子２１０をインナーリード２３１とともに樹脂固定用テープ２７０上に固定した状態で，ワイヤボンディング工程を行い，樹脂封止しているである．尚，樹脂封止後のプレスによる不要部分の切断工程の形成は，実施例１と同様である．図１０（ａ）に示すリードフレーム２３０Ａを得るには，図９（ａ）に示すリードフレーム１３０Ａを得た場合と同様にしてある．即ち，図１０（ｂ）に示すエッチングにより形成された後のものものであり，図１０（ａ）に示す形状にするための，図１０（ｃ），（Ｃ）に示すように，基本，成形のため樹脂テープ２６０（ポリイミドテープ）を使用する．

【００２１】図５（ａ）～図５（ｃ）に，実施例２の半導体装置の変形例半導体装置の断面図である．図５（ａ）に示す変形例半導体装置は，半導体素子の向きが図５（ａ）で，気密封を行する面を下側にしている点，およびワイヤボンディング後をリードフレームの第１面に設けてモールドで実施例２の半導体装置と異なる点を図５（ｂ），図５（ｃ）に示す変形例半導体装置は，それぞれ実施例２の半導体装置，図５（ａ）に示す変形例の半導体装置において，半球状の半田からなる吊下部を設けず，端子部の底を接続端子部として用いているものである．樹脂封がなく，吊下ピン２３３の側面２３３Ｂを外部に露出しているため，テスタ等での信号のチェックがしやすい構造となっている．

【００２２】次いで，実施例３の樹脂封止型半導体装置を説明する．図６（ａ）に実施例３の樹脂封止型半導体装置の断面図であり，図６（ｂ）に図６（ａ）のＡ５－Ａ６におけるインナーリード部の断面図で，図６（ｃ）に図６（ａ）のＳ５－Ｂ６における吊下ピン部の断面図である．尚，実施例３の半導体装置の外観は実施例１とほぼ同じとなるため，図は省略した．図６中，３００は半導体装置，３１０は半導体素子，３１２はバンプ，３３０はリードフレーム，３３１はインナーリード，３３１Ａａは第１面，３３１Ａｂは第２面，３３１Ａｃは第３面，３３１Ａｄは第４面，３３３は吊下ピン部，３３３Ａは接手部，３３３Ｂは側面，３３３Ｓは上端面，３４０は

封止用テープである．本実施例３の半導体装置においては，半導体素子３１０は，バンプ３１１によりインナーリード３３１の第２面３３１Ａｂに固定され，さらにインナーリード３３１と接続している．リードフレーム３３０は，図１０（ａ），図１０（ｂ）に示す形のもので，図１１に示すエッチング加工により形成されたものを用いている．図１３（ｃ）（ｂ）に示すように，インナーリード３３１の幅方向の長さＷＩＡ，Ｗ２Ａ（約１００μｍ）ともこの長方向の幅寸法Ｗａよりも大きくなっており，且つ，インナーリード３３１の第２面３３１Ａｂにインナーリードの内側に向かって凹んだ形状で，第１面３３１Ａａが広くなることより，インナーリードの微細化に対応できるとともに，インナーリード３３１の第２面３３１Ａにおいて，半導体素子とバンプにて接続するために接続する際には，図１３（ｃ）（ｂ）のように接続がしやすいものとしている．また，本実施例３の場合も，実施例１や実施例２の場合と同様に，半導体装置３００と放熱板との電気的な接続は，吊下ピン３３３先端部に設けられた半球状の半田からなる接手部３３３Ａを介してプリント基板等へ接続されることにより行われる．

【００２３】実施例３の半導体装置は，実施例１の半導体装置の場合とほぼ同様，図１２に示すエッチングにより所定形状に形成されたリードフレームを用いたものであるが，半導体装置Ｂ面の接続方法にほぼ同じ工程である．異なる点は，実施例１の半導体装置の場合には半導体素子もインナーリードに固定した状態でワイヤボンディングを行い，樹脂封止しているのに対し，本実施例３の半導体装置の場合には，半導体素子３１０もインナーリード３３１にバンプを介して固定して電気的に接続した状態で樹脂封止している点である点，樹脂封止後のプレスによる不要部分の切断，端子形状の形成は，実施例１の半導体装置の場合と同じである．

【００２４】図６（ａ）に，実施例３の半導体装置の変形例半導体装置の断面図である．図６（ａ）に示す変形例半導体装置は，実施例３の半導体装置において，半球状の半田からなる吊下部を設けず，端子部の底を接続端子として用いているものである．樹脂封を無くして吊下ピン３３３の側面３３３Ｂを外部に露出しているため，テスタ等での信号のチェックがしやすい構造となっている．更にこの吊下ピン３３３の側面３３３Ｂを外部に露出させることにより，外部からチェックしやすい構造とすることもできる．

【００２５】次いで，実施例４の樹脂封止型半導体装置を説明する．図７（ａ）に実施例４の樹脂封止型半導体装置の断面図であり，図７（ｂ）に図７（ａ）のＡ７－Ａ８におけるインナーリード部の断面図で，図６（ｃ）に図６（ａ）のＢ７－Ｂ８における吊下ピン部の断面図である．尚，実施例４の半導体装置の外観は実施例１とほぼ同じとなるため，図は省略した．図７中，５００は半導体装置，４１０は半導体素子，４１１はバンド，４３０は

リードフレーム，４３１はインナーリード，４３１Ａａは第１面，４３１Ａｂは第２面，４３１Ａｃは第３面，４３１Ａｄは第４面，４３３は半田ボール，４３３Ａは半田，４３３Ｂは銀面，４３３Ｓは上面，４４０は封止用樹脂，４７０は絶縁性接着材である．本実施例の場合は，半導体チップ４１０のパッド３１１側の面をインナーリード３３１の第２面４３１Ａｂに絶縁性接着材４７０を介して固定し，パッド４１１とインナーリード４３１の第１面４３１Ａａとをワイヤ４２０にて電気的に接続したものである．図示するリードフレームは実施例３と同じ．図１０（ａ），図１０（ｂ）に示すＱＦＰ形状のものを使用している．また，本実施例４の場合も，実施例１や実施例２の場合と同様に，半導体装置４００と外部回路との電気的な接続は，球状ボール３３３先端部に設けられた半田材の半田からなる球状半田４３３Ａを介してプリント基板等へ接続されることにより行われる．

【００２６】図７（ｃ）は，実施例４の半導体装置の変形例や参考例の断面図である．図７（ｃ）に示す変形例や参考例の場合は，実施例４の半導体装置において，ニッケルの二回からなる球状半田を設けず，球状ボールの表面を半田部として用いているものである．この場合も，前述した球状ボール４３３の側面４３３Ｂを側面に露出している．テスタ等での信号のテストがしやすい構造となっている．

【００２７】

【発明の効果】本発明の樹脂封止型半導体装置は，上記のように，リードフレームを用いた樹脂封止型半導体装置において，多端子化に対応でき，且つ，従来の図１３（ｂ）に示すアウターリードを持つリードフレームを用いた場合のようにダムバーのカット工程や，ダムバーの曲げ工程を必要としない．即ち，アウターリードのスキューの問題や平坦性（コープラナリティー）の問題を考慮せずに半導体装置の信頼性を可能としている．また，ＱＦＰやＢＧＡに比べるとパッケージ内部の反りが起こりにくくなるため，封止樹脂が少なくなり半導体装置Ｍを軽くすることを可能にしている．

【図面の簡単な説明】

【図１】実施例１の樹脂封止型半導体装置の断面図

【図２】実施例１の樹脂封止型半導体装置の底面及び平面図

【図３】実施例１の樹脂封止型半導体装置の変形例の断面図

【図４】実施例２の樹脂封止型半導体装置の断面図

【図５】実施例２の樹脂封止型半導体装置の変形例の断面図

【図６】実施例３の樹脂封止型半導体装置の断面図

【図７】実施例４の樹脂封止型半導体装置の断面図

【図８】実施例１の樹脂封止型半導体装置のにごりを説明するための図

【図９】本発明の樹脂封止型半導体装置に用いられるリードフレームの図

【図１０】本発明の樹脂封止型半導体装置に用いられるリードフレームの図

【図１１】本発明の樹脂封止型半導体装置に用いるリードフレームの作製方法を説明するための図

【図１２】本発明の樹脂封止型半導体装置に用いるリードフレームの作製方法を説明するための図

【図１３】インナーリード先端部でのワイボンディングの高信頼性を示す図

【図１４】従来のリードフレームのニッケルニ回メッキを説明するための図

【図１５】本発明封止型半導体装置及び実施リードフレームの図

【符号の説明】

１００．２００．３００．４００　本発明封止型半導体装置

１１０．２１０．３１０．４１０　半導体チップ

１１１．２１１．４１１　電極（パッド）

３１２　ワイヤボンディング

１２０．２２０．４２０　ワイヤ

１２０Ａ．１２０Ｂ　ワイヤ

Ｌ２１Ａ．Ｌ２１Ｂ　めっき層

１３０．２３０．３３０．４３０　リードフレーム

１３１．２３１．３３１．４３１　インナーリード

１３１Ａａ．２３１Ａａ．３３１Ａａ．４３１Ａａ　第１面

１３１Ａｂ．２３１Ａｂ．３３１Ａｂ．４３１Ａｂ　第２面

１３１Ａｃ．２３１Ａｃ．３３１Ａｃ．４３１Ａｃ　第３面

１３１Ａｃ．２３１Ａｄ．３３１Ａｃ．４３１Ａｄ　第４面

１３１Ｂ　電極

１３３．２３３．３３３．４３３　半田

１３３Ａ．２３３Ａ．３３３Ａ．４３３Ａ　半田

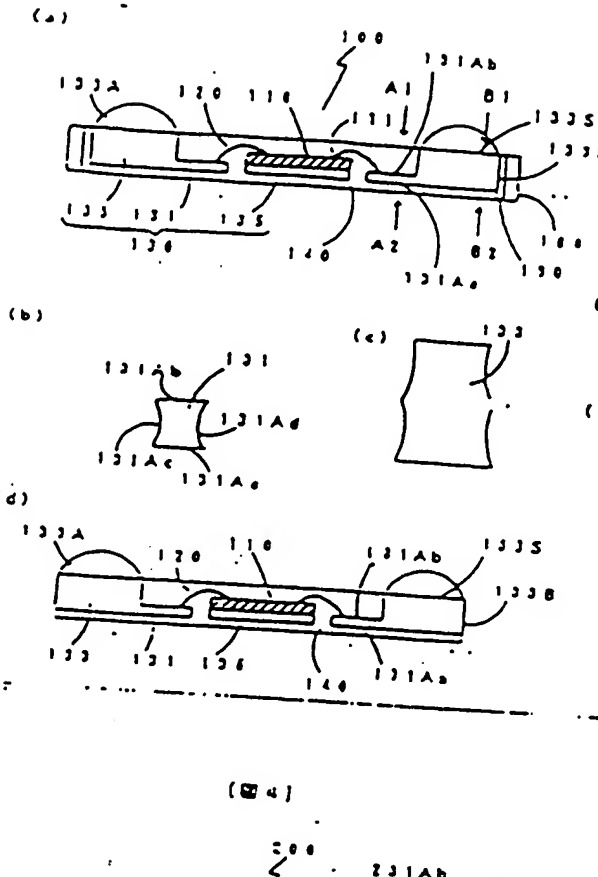
１３３Ｂ．２３３Ｂ．３３３Ｂ．４３３Ｂ　側面

１３３Ｓ．２３３Ｓ．３３３Ｓ．４３３Ｓ　上面

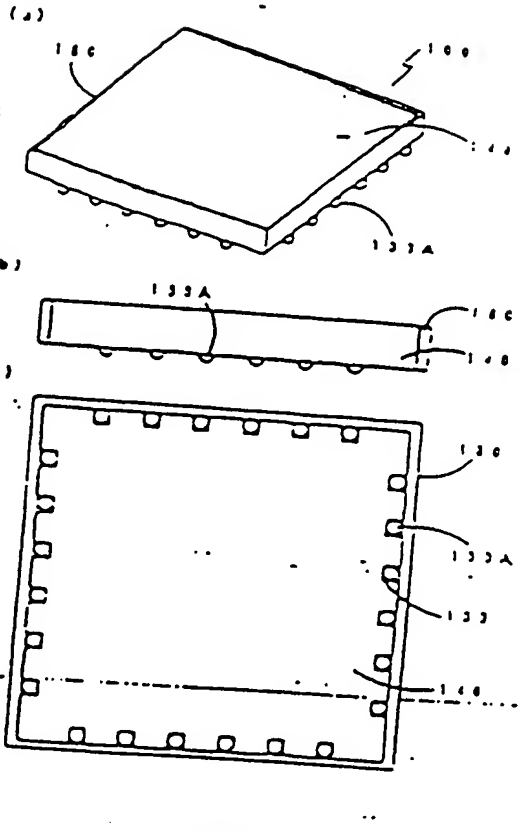
１４０．２４０．３４０．４４０　封止用樹脂

１５０　銀

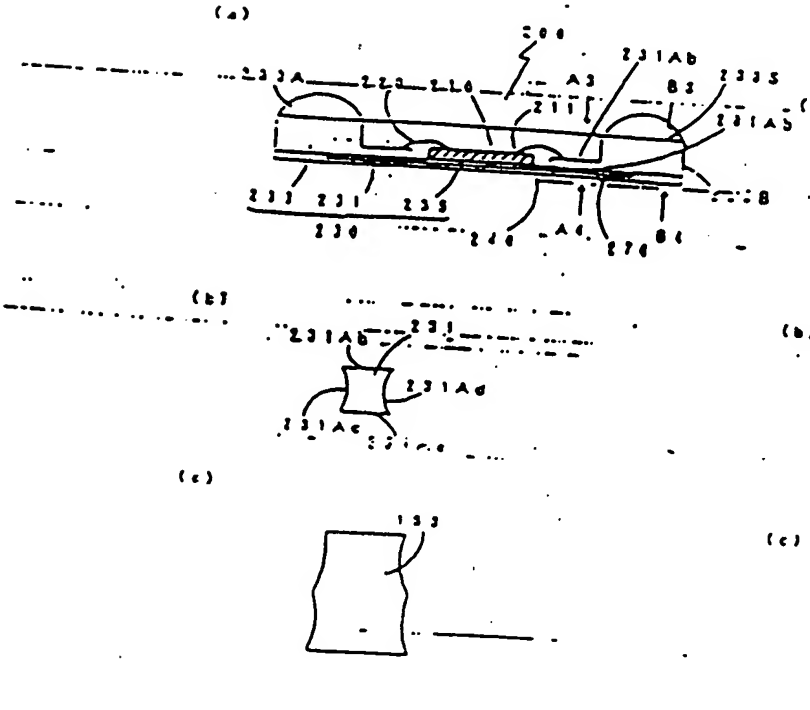
(図1)


(a)
100
131Ab
133A
120
110
A1
B1
133S
133B
133
131
135
130
140
A2
B2
131Aa
150
(b)
131Ab
131
131Ad
131Ac
131Aa
(c)
133
(d)
133A
120
110
131Ab
133S
133B
133
131
135
130
140
131Ab

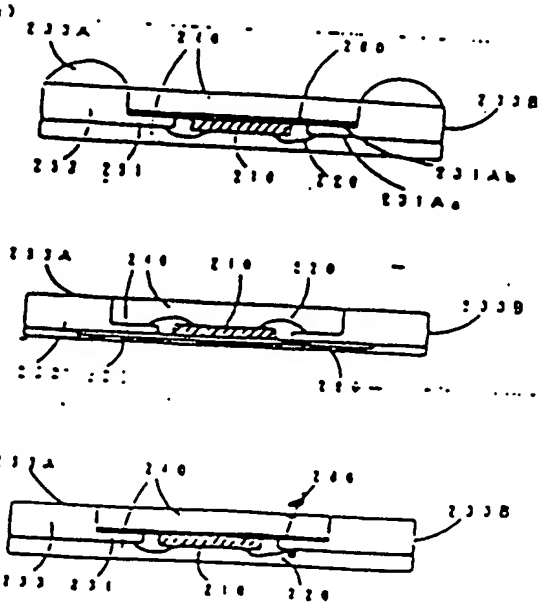
(図2)


(a)
150
100
140
133A
(b)
133A
150
140
(c)
130
133A
133
140

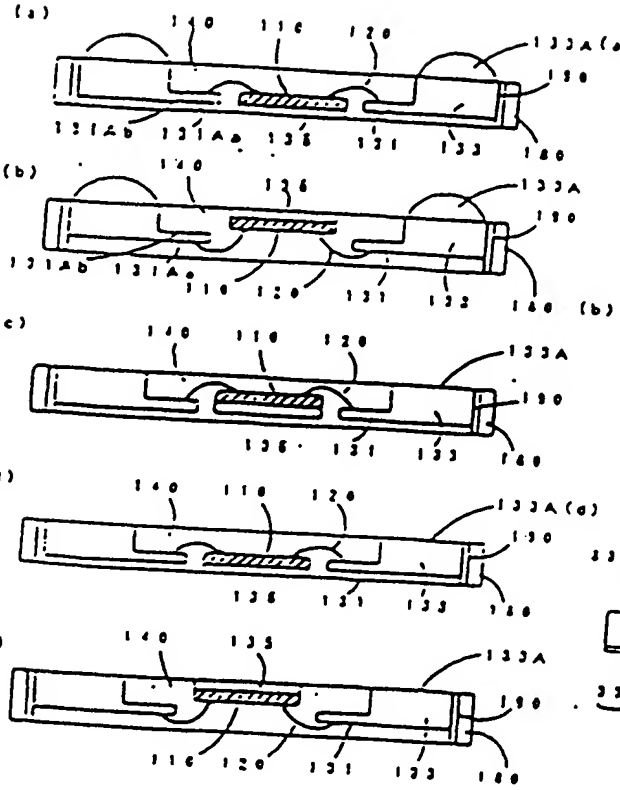
(図4)


(a)
200
231Ab
233A
220
210
A3
B3
233S
231Aa
233
231
235
230
240
A4
270
B4
B
(b)
231Ab
231
231Ad
231Ac
(c)
133

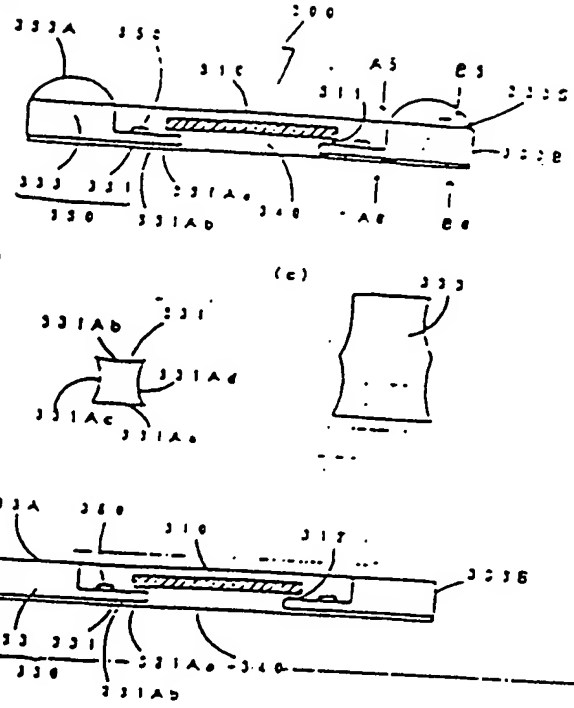
(図5)


(a)
233A
210
220
233B
232
231
231Ab
231Aa
(b)
233A
240
210
220
233B
(c)
233A
240
210
233B
233
231
210
220

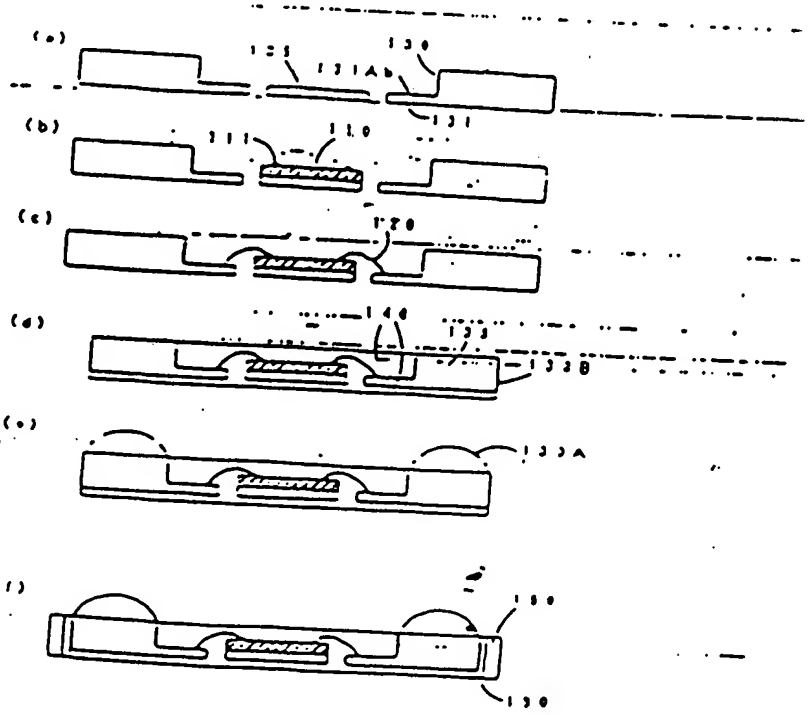
(図3)


(a)
140
110
120
133A(a)
150
131Ab
131Aa
135
131
133
160
(b)
140
135
133A
150
131Ab
131Aa
110
120
131
133
160
(c)
140
110
120
133A
150
135
131
133
160
(d)
140
110
120
133A(d)
150
135
131
133
160
(e)
140
135
133A
150
110
120
131
133
160

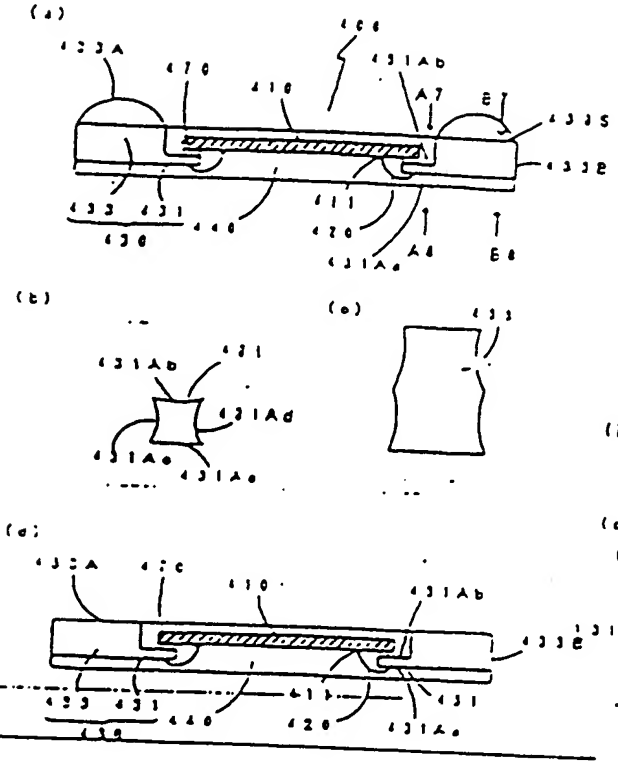
(図6)


300
333A
335
311
AS
es
333C
333B
333
331
330
331Ab
331Aa
340
As
es
(b)
331Ab
331
331Ad
331Ac
331Aa
(c)
333
333A
350
310
317
333B
333
331
330
331Aa
340
331Ab

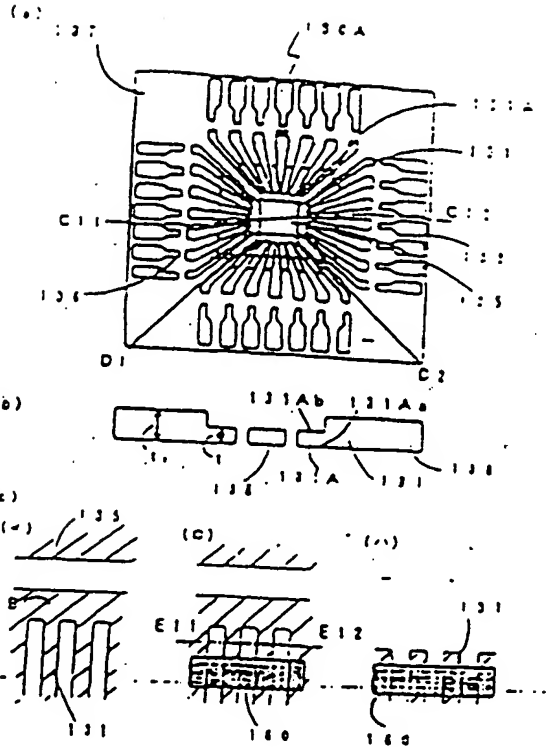
(図8)


(a)
135
131Ab
130
131
(b)
111
110
(c)
120
(d)
140
133
133B
(e)
133A
(f)
150
130

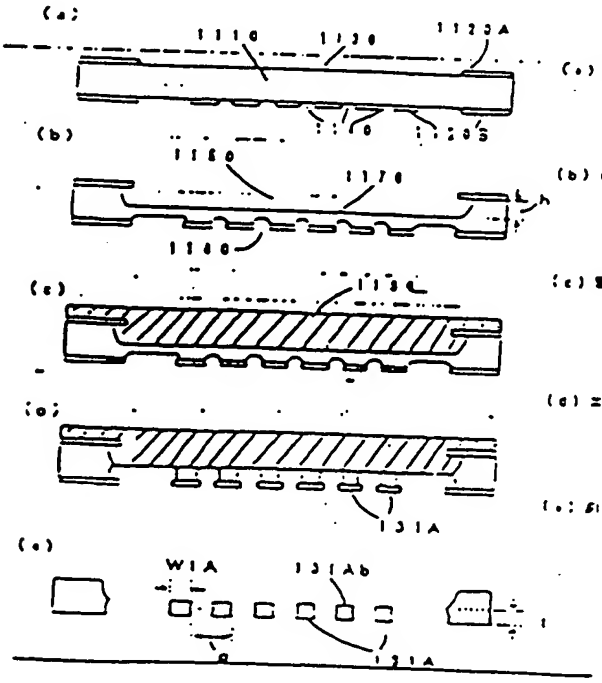
(図7)


(a)
433A
470
410
431Ab
A7
E7
433S
433B
433
431
430
440
411
420
431Aa
A8
E8
(b)
431Ab
431
431Ad
431Ac
431Ae
(c)
433
(d)
433A
410
431Ab
433B
433
431
430
440
411
420
431Aa

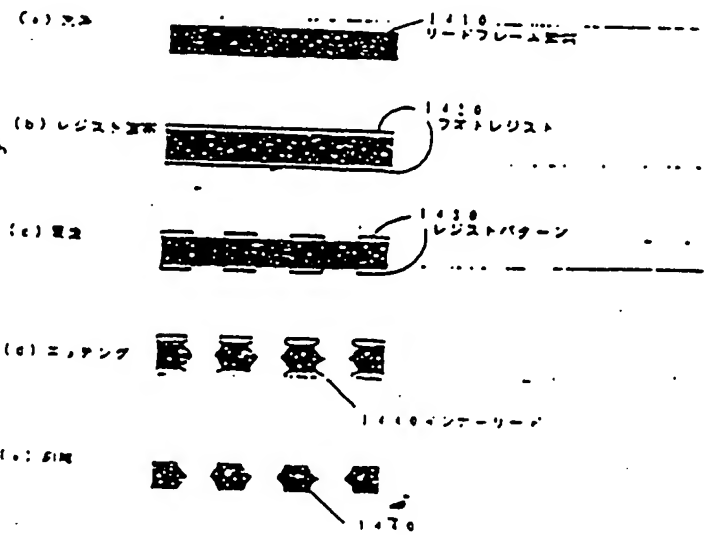
(図9)


(a)
137
135A
131A
131
C11
C12
132
136
135
D1
D2
(b)
131Ab
131Aa
138
131A
131
(c)
(イ)
135
131B
(ロ)
(ハ)
E11
E12
131
131
160
160

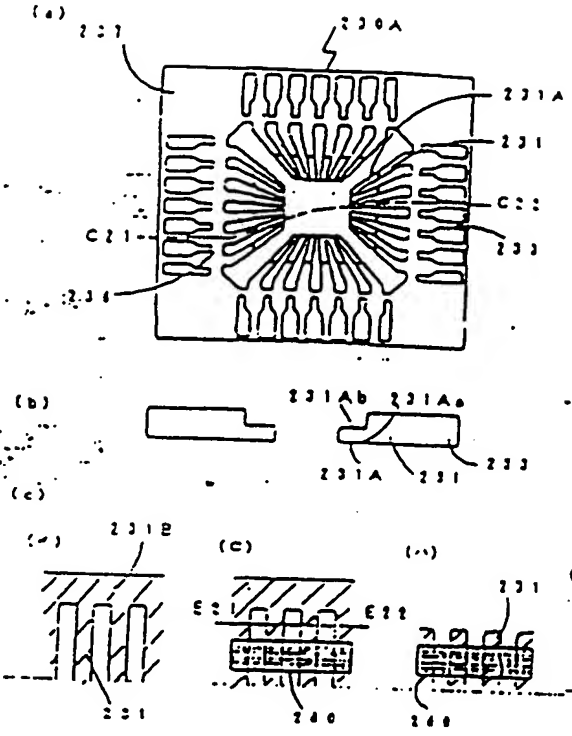
(図11)


(a)
1110
1130
1120A
1120
1120S
(b)
1150
1170
1160
(c)
1130
(d)
131A
(e)
W1A
131Ab
131A

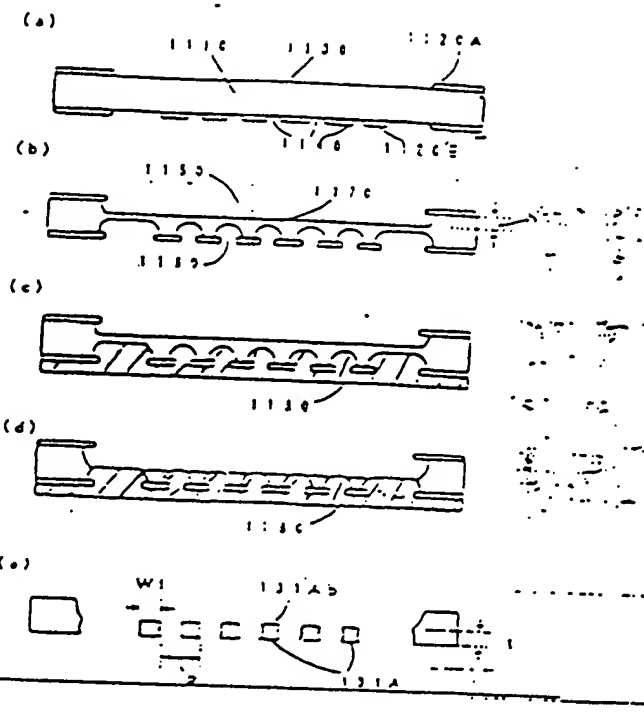
(図14)


(a) マスク
1410
リードフレーム基材
(b) レジスト塗布
1420
ウエトレジスト
(c) 露光
1430
レジストパターン
(d) エッチング
1440インナーリード
(e) 剥離
1470

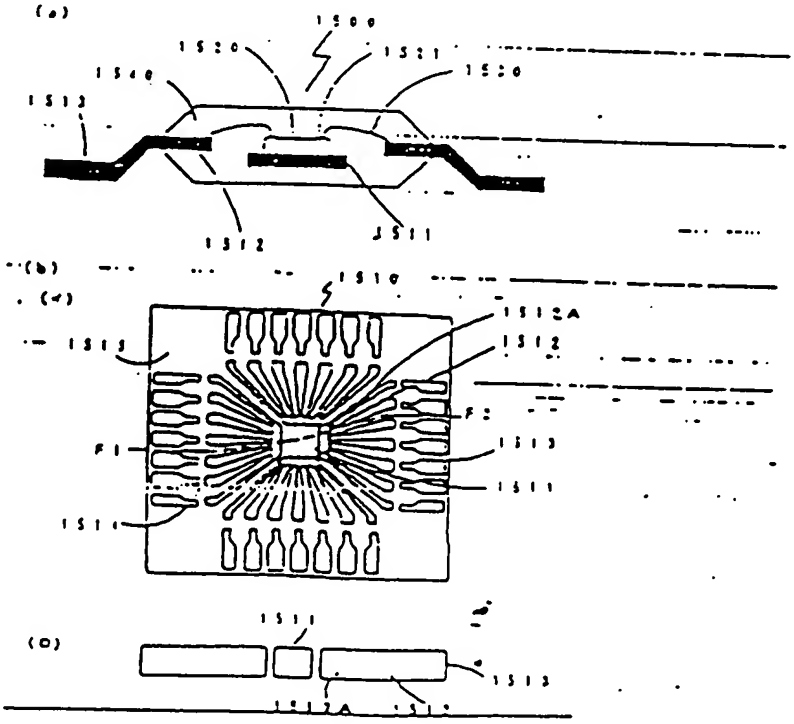
【図10】


(a)
231
230A
231A
231
C22
C21
233
234
(b)
231Ab
231Aa
231A
231
233
(c)
231B
(c)
(d)
231
E21
E22
231
231
240
240

【図12】


(a)
1110
1130
1120A
1140
1120B
(b)
1150
1170
1160
(c)
1130
(d)
1180
(e)
W1
131Ab
131A

【図15】


(a)
1500
1520
1521
1530
1540
1513
1512
1511
(b)
(c)
1510
1512A
1512
1513
F2
F1
1513
1511
1514
(d)
1511
1513
1512A
1512

第13図